METHOD AND STRUCTURE TO IMPROVE THE GATE COUPLING RATIO (GCR) FOR MANUFACTURING A FLASH MEMORY DEVICE

ABSTRACT OF THE INVENTION

Method and structure to improve the gate coupling ratio (GCR) for manufacturing a flash memory device are provided. The method and structure include the following steps. A gate oxide layer, a first semiconductor layer, and an insulating layer are formed sequentially over a provided semiconductor substrate. An etching process is used to etch the insulating layer. A semiconductor spacer is then deposited and used as a self-aligned etching mask. After the self-aligned etching, the insulating layer is removed and an insulating stacked structure is deposited. Finally, a second semiconductor layer is deposited and etched to form the control gate region.